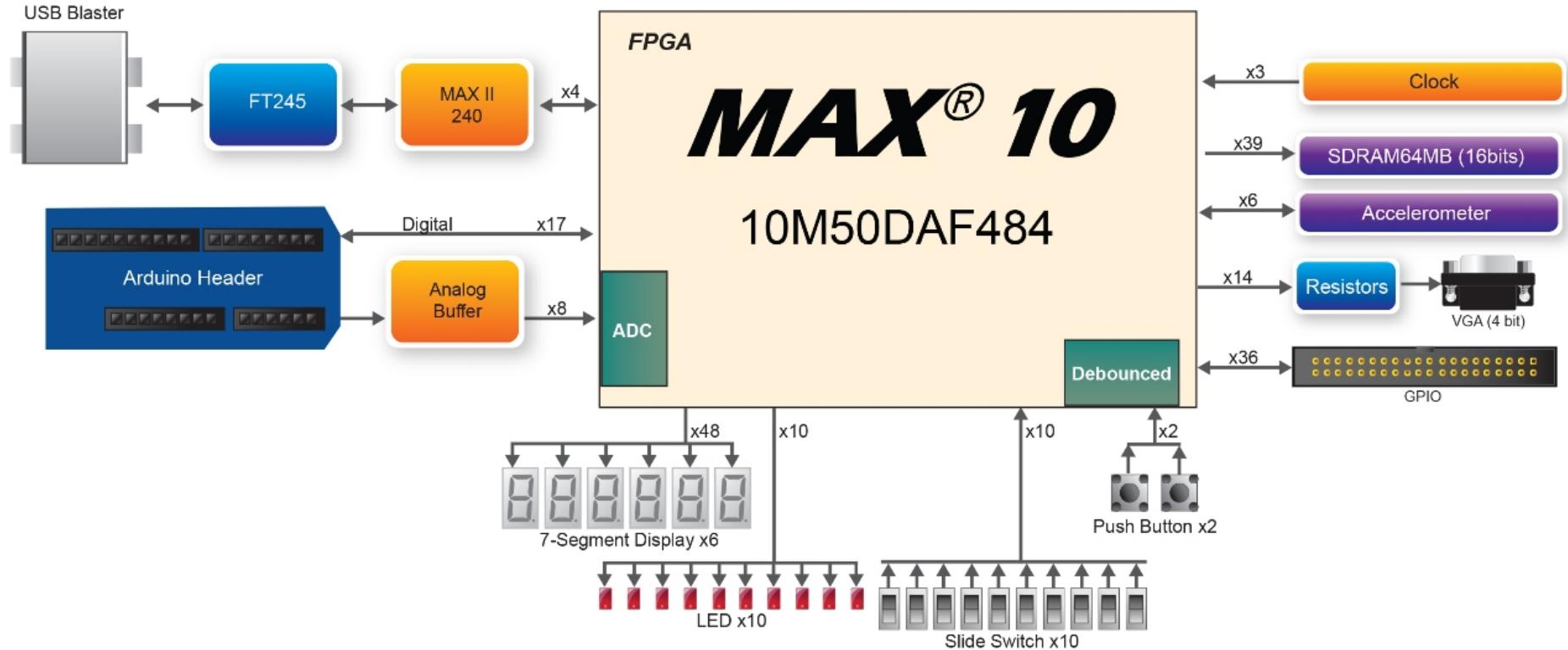


# ALTERA MAX10 Development & Education Board (DE10-Lite)

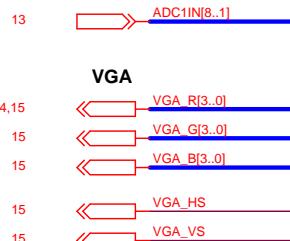
PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	19	
2	Block Diagram	20	
3	MAX 10 Bank 1 & 2	21	
4	MAX 10 Bank 3 & 4	22	
5	MAX 10 Bank 5 & 6	23	
6	MAX 10 Bank 7 & 8	24	
7	MAX 10 Clocks	25	
8	MAX 10 Configuration	26	
9	MAX10 Power		
10	MAX10 Ground		
11	MAX10 Decoupling		
12	SDRAM		
13	GPIO and Arduino Interface		
14	LED, 7'Seg, User IO		
15	VGA and Accelerometer		
16	Power - 5V, 1.2V		
17	Power - 1.8V, 2.5V, 3.3V		
18	USB Blaster		



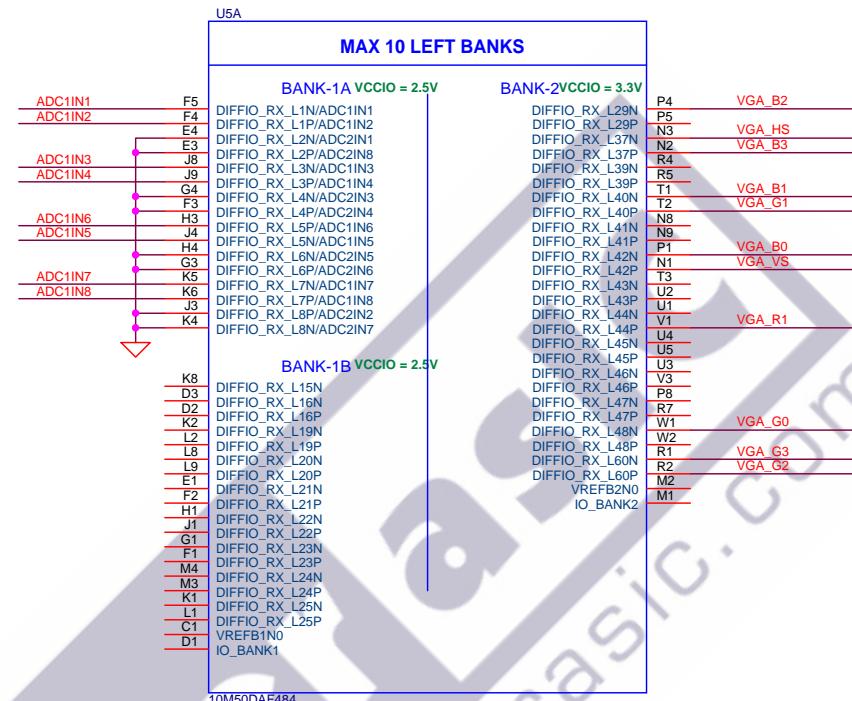
terasic DESIGN YOUR WORLD		
Copyright © 2017 by Terasic Inc. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
<b>Title</b> <b>DE10-Lite</b>		
<b>Size</b> <b>B</b>	<b>Document Number</b> <b>Block Diagram</b>	<b>Rev</b> <b>E0</b>
<b>Date:</b> Thursday, April 13, 2017	<b>Sheet</b> 1	<b>2 of 18</b>

# MAX10 Bank 1 & 2

## Analog input interface



## VGA



		Copyright © 2017 by Terasic Inc. Terasic. All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		DE10-Lite
Size	Document Number	Rev
B	MAX 10 Bank 1 & 2	E0
Date:	Friday, August 11, 2017	Sheet
	1	3 of 18

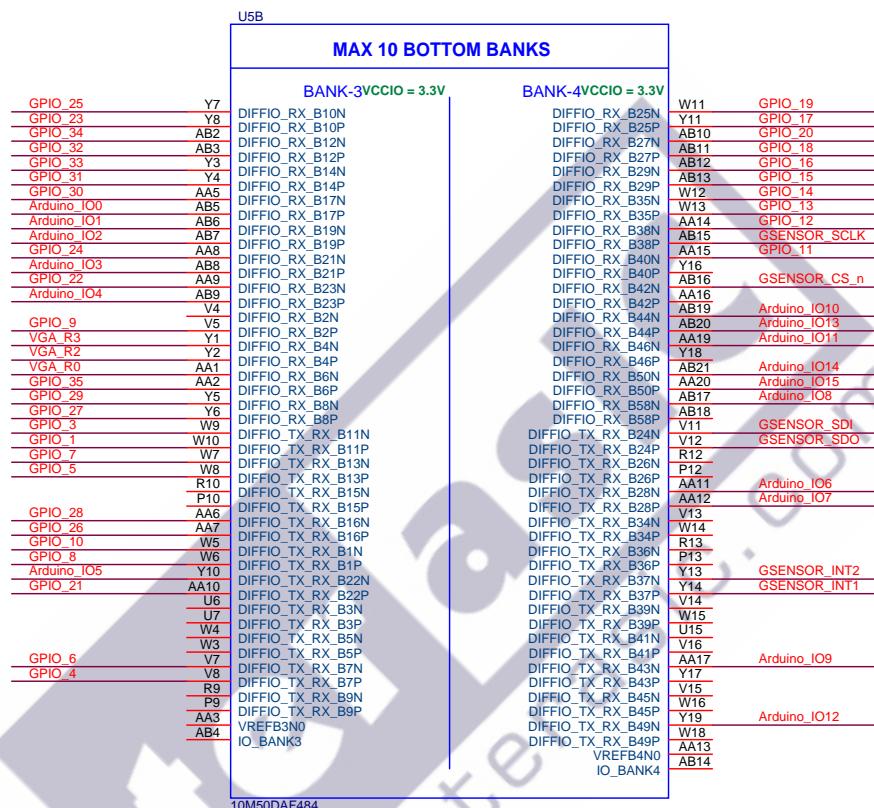
# MAX10 Bank 3 & 4

**GPIO 0**  
7,13      GPIO [35..0]

**Arduino Digital Interface**  
13      Arduino IO[15..0]

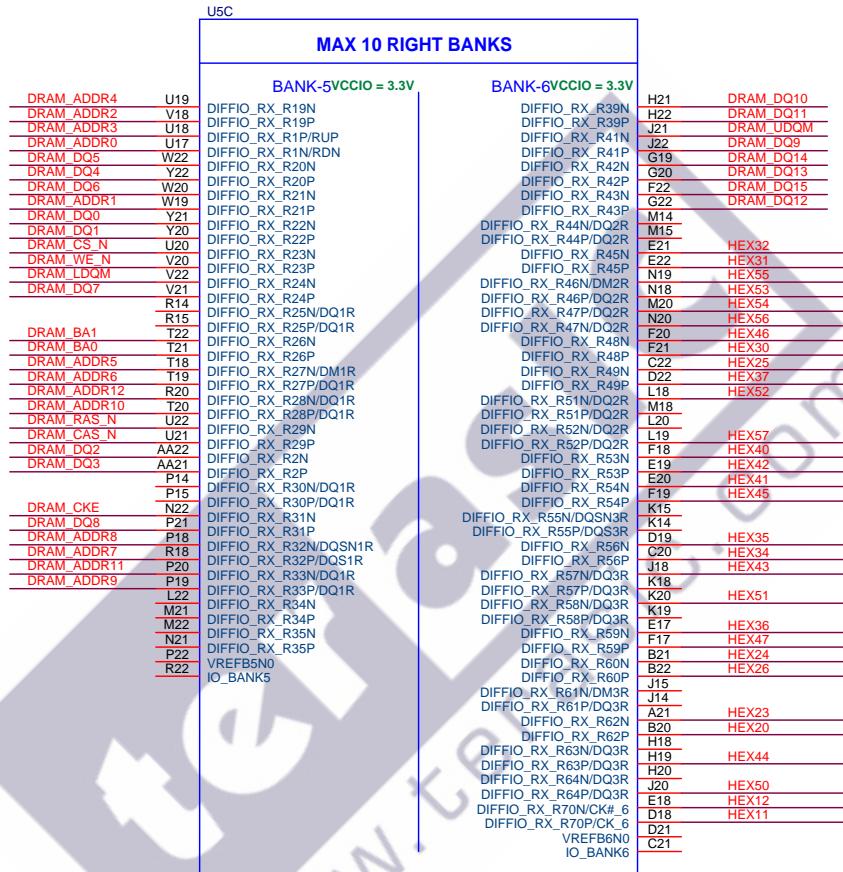
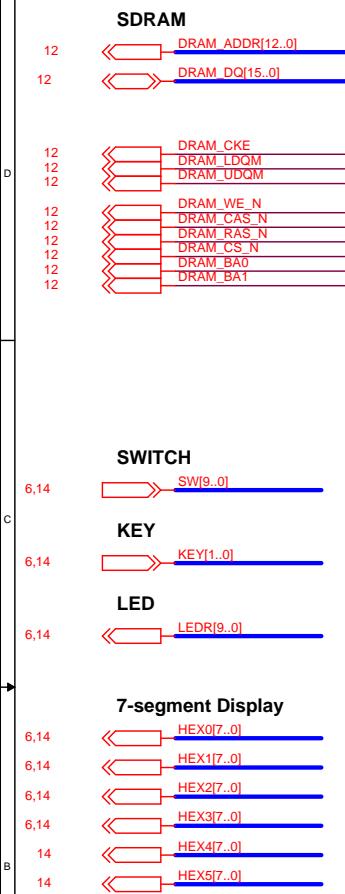
**Digital Accelerometer**  
15      GSENSOR\_SDI  
15      GSENSOR\_SCLK  
15      GSENSOR\_INT1  
15      GSENSOR\_INT2  
15      GSENSOR\_CS\_n  
15      GSENSOR\_SDO

**VGA**  
3,15      VGA\_R[3..0]



<b>terasic</b>		Copyright © 2017 by Terasic Inc. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title		DE10-Lite
Document Number		
Size	MAX 10 Bank 3 & 4	Rev
B		E0
Date:	Friday, August 11, 2017	Sheet
	1	4 of 18

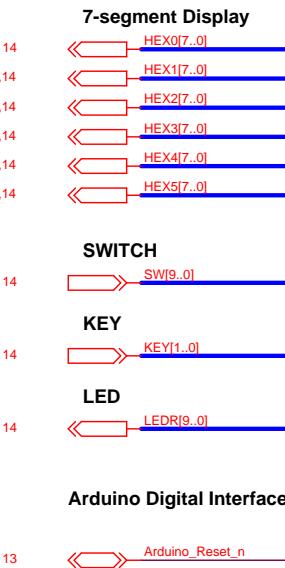
# MAX10 Bank 5 & 6



**terasic** Copyright © 2017 by Terasic Inc. All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
DE10-Lite		
Size	Document Number	Rev
B	MAX 10 Bank 5 & 6	E0
Date:	Friday, August 11, 2017	Sheet
		5 of 18

MAX10 Bank 7 & 8



Copyright (c) 2017 by Terasic Inc. All rights reserved.

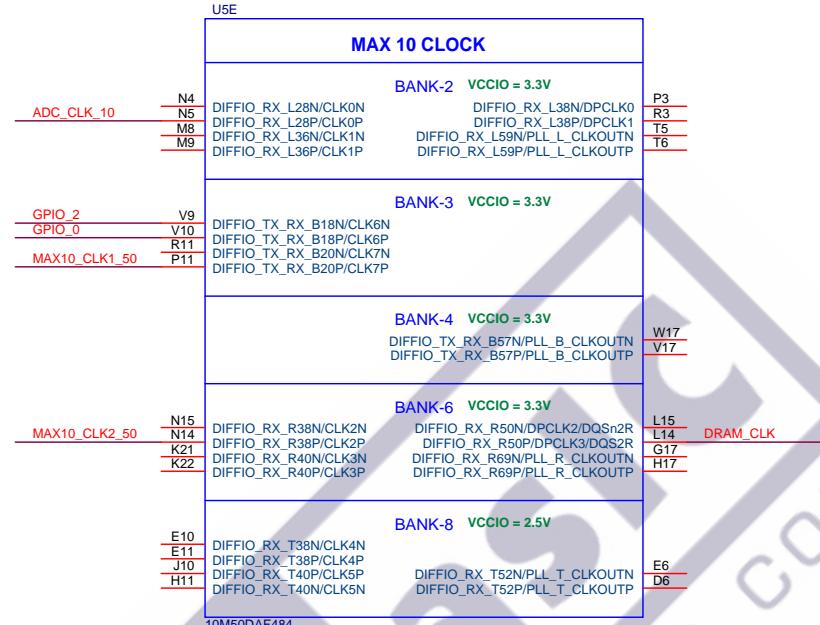
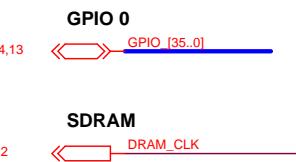
part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

**Title**

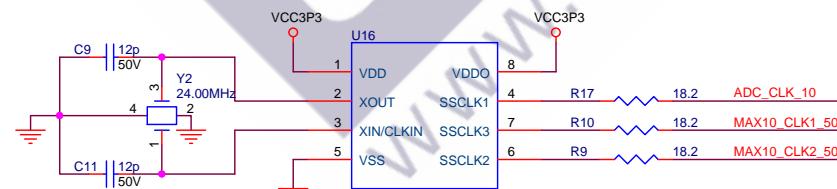
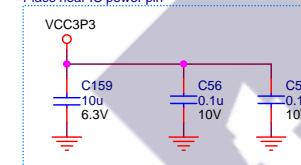
DE10-Lite

Size B	Document Number MAX 10 Bank 7 & 8	Rev E0
Date:	Friday, August 11, 2017	Sheet 6 of 18

# MAX10 Clock



CAD Note:  
Place near IC power pin



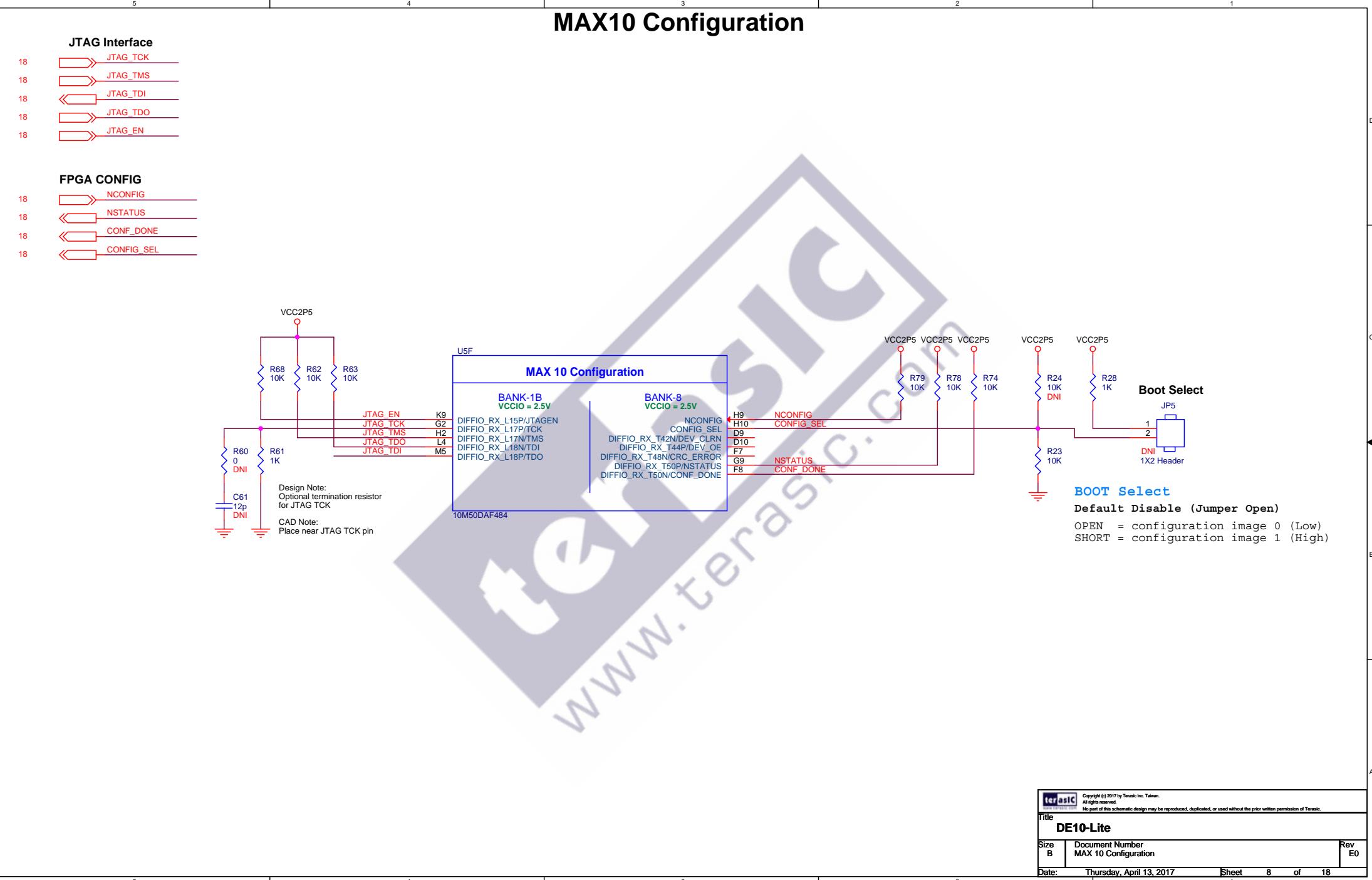
terasic

Copyright © 2017 by Terasic Inc. All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

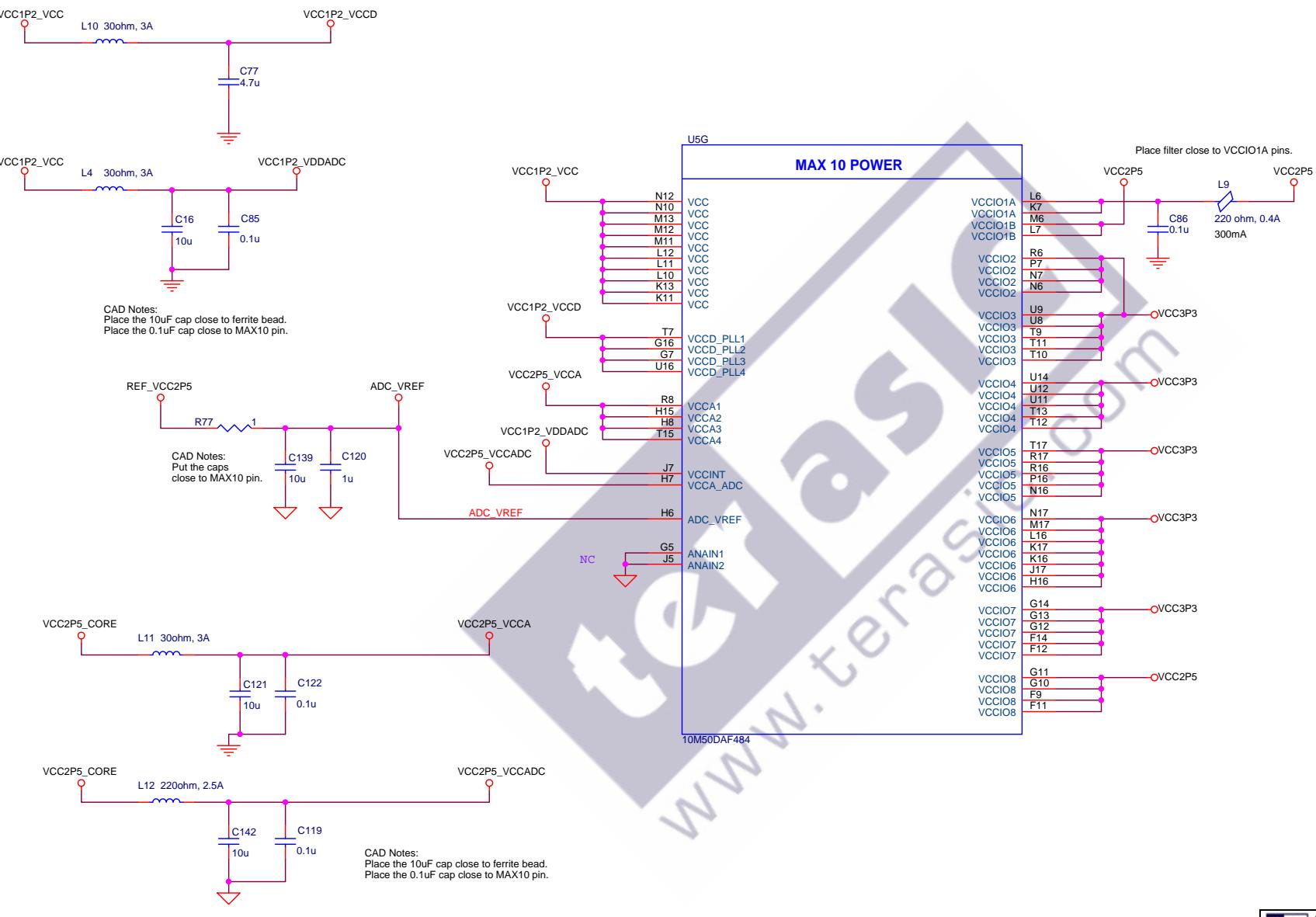
**Title** DE10-Lite

<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
B	MAX 10 Clocks	E0
<b>Date:</b> Friday, August 11, 2017		<b>Sheet</b> 1
7 of 18		

# MAX10 Configuration

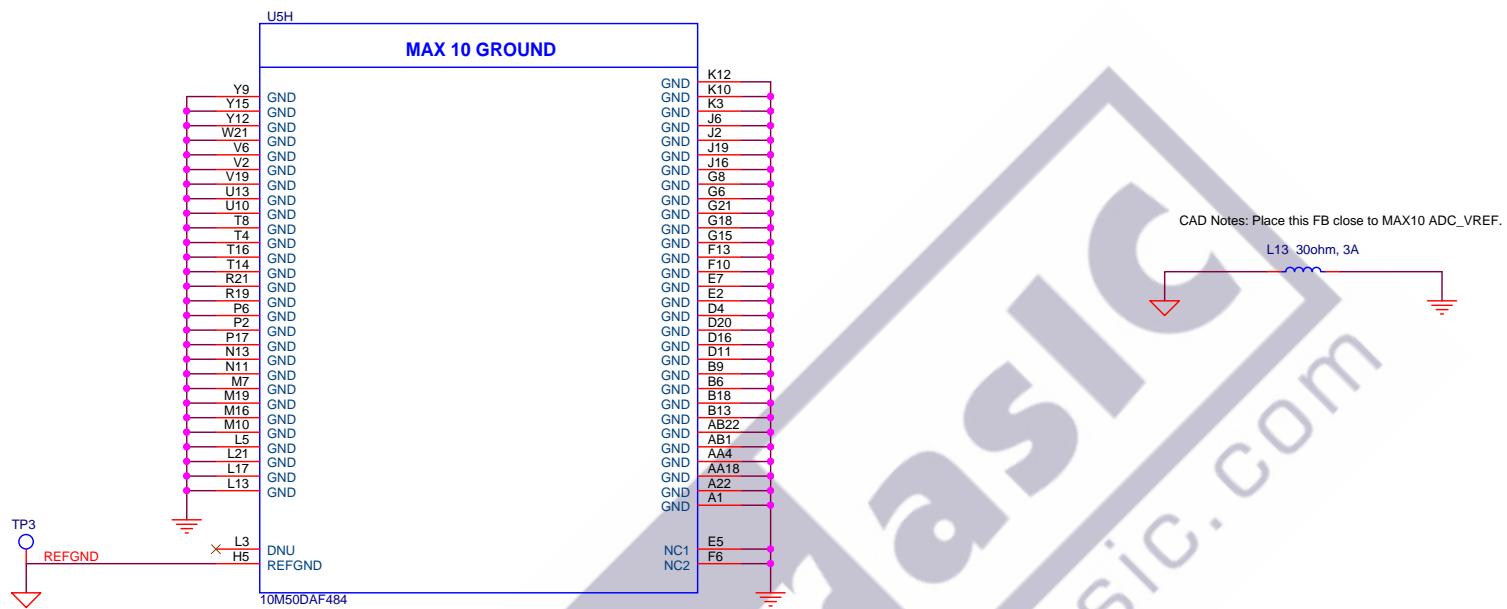


# MAX10 Power



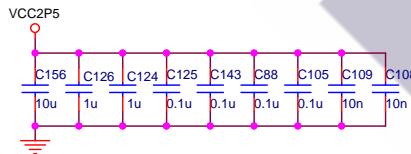
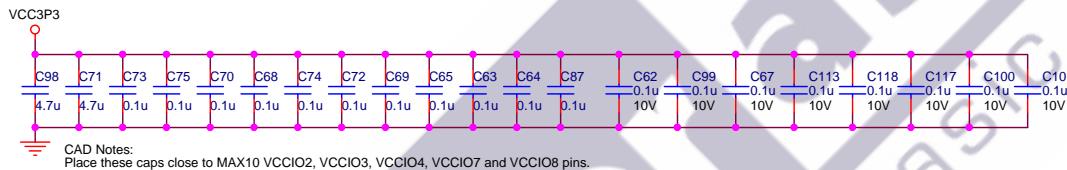
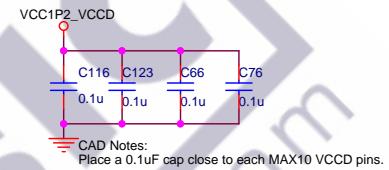
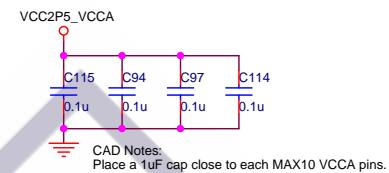
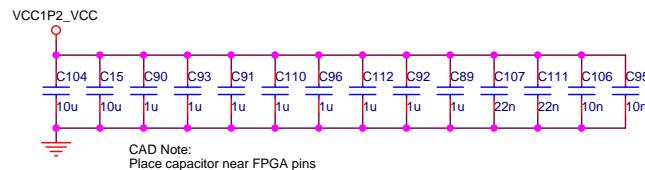
		Copyright © 2017 by Terasic Inc. Terasic. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title		DE10-Lite
Size	Document Number	Rev
B	MAX10 Power	E0
Date:	Thursday, April 13, 2017	Sheet
	1	9 of 18

# MAX10 Ground



terasic		
Copyright © 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title DE10-Lite		
Size B	Document Number MAX10 Ground	Rev E0
Date: Thursday, April 13, 2017	Sheet 1	10 of 18

# MAX10 Decoupling

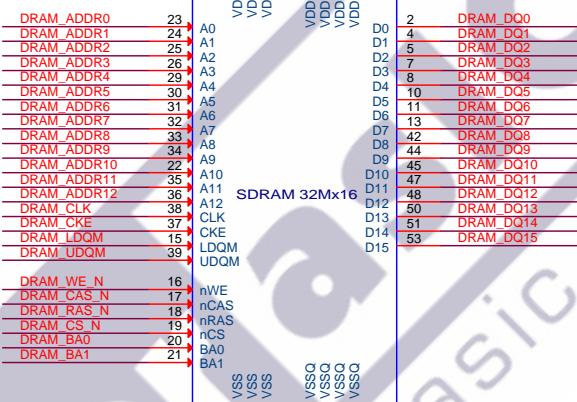
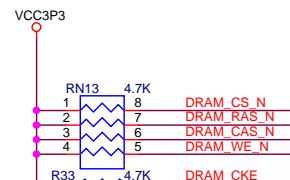


terasic DESIGN YOUR WORLD		
Copyright © 2017 by Terasic Inc. Terasic. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
<b>Title</b>		
<b>DE10-Lite</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
B	MAX10 Decoupling	E0
Date:	Thursday, April 13, 2017	Sheet
	1	11 of 18

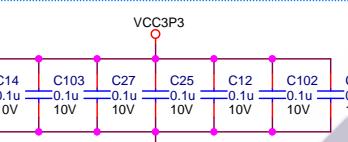
**SDRAM**

5 DRAM\_ADDR[12..0]  
 5 DRAM\_DQ[15..0]

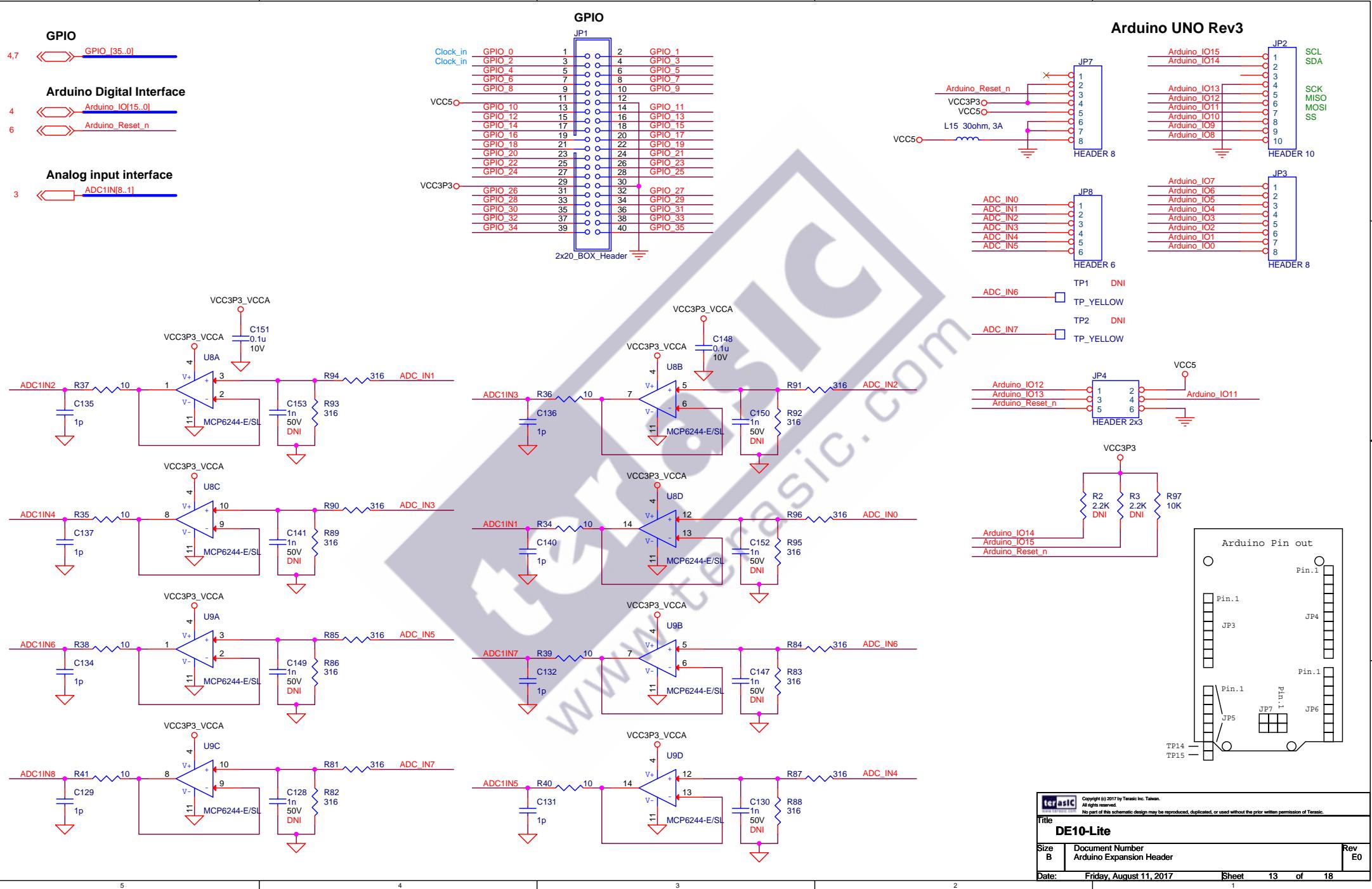
7 DRAM\_CLK  
 5 DRAM\_CKE  
 5 DRAM\_LDQM  
 5 DRAM\_UDQM  
 5 DRAM\_WE\_N  
 5 DRAM\_CS\_N  
 5 DRAM\_RAS\_N  
 5 DRAM\_CS\_N  
 5 DRAM\_BA0  
 5 DRAM\_BA1



CAD Note:  
 Place near IC power pin



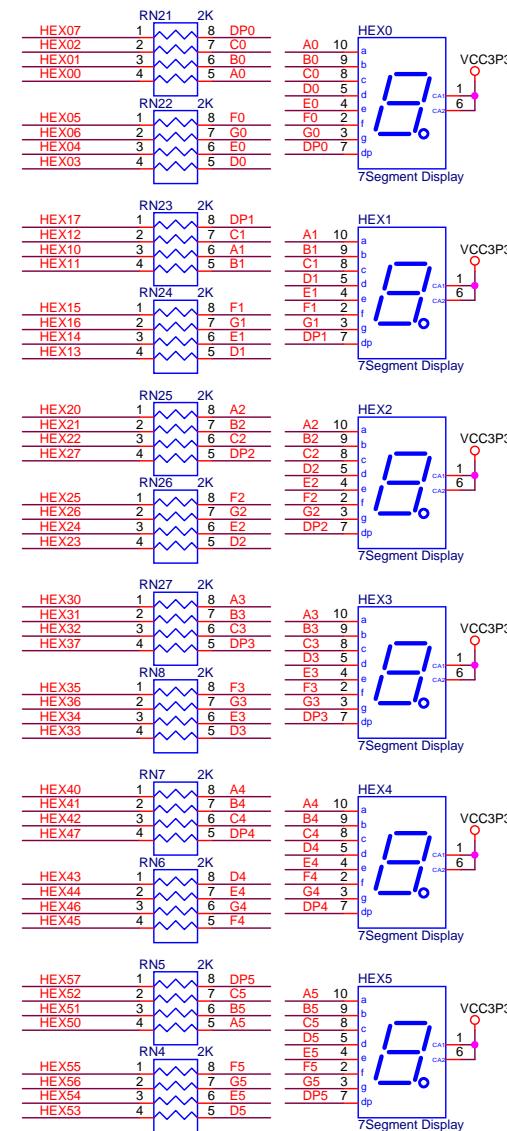
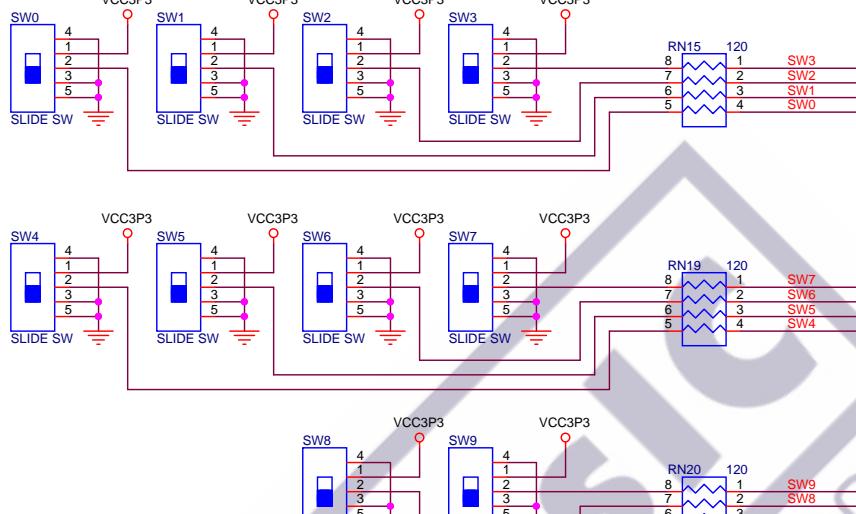
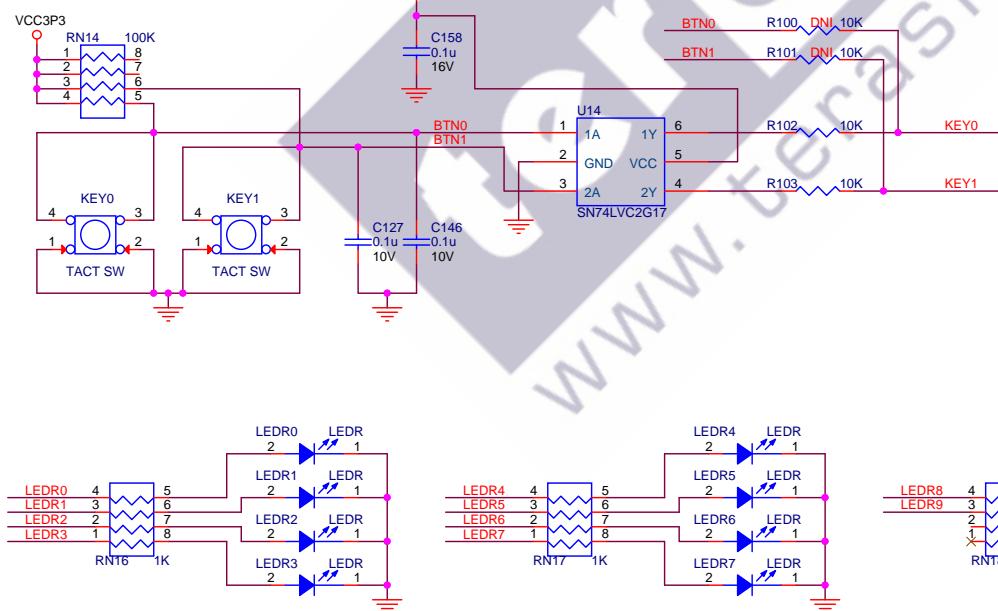
 <b>DE10-Lite</b>		Copyright © 2017 by Terasic Inc. All rights reserved.	
		No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
<b>Title</b>	<b>DE10-Lite</b>	<b>Size</b>	<b>Document Number</b>
B	SDRAM	E0	
<b>Date:</b>	Thursday, April 13, 2017	<b>Sheet</b>	12 of 18



# User IO, 7-Seg, LED

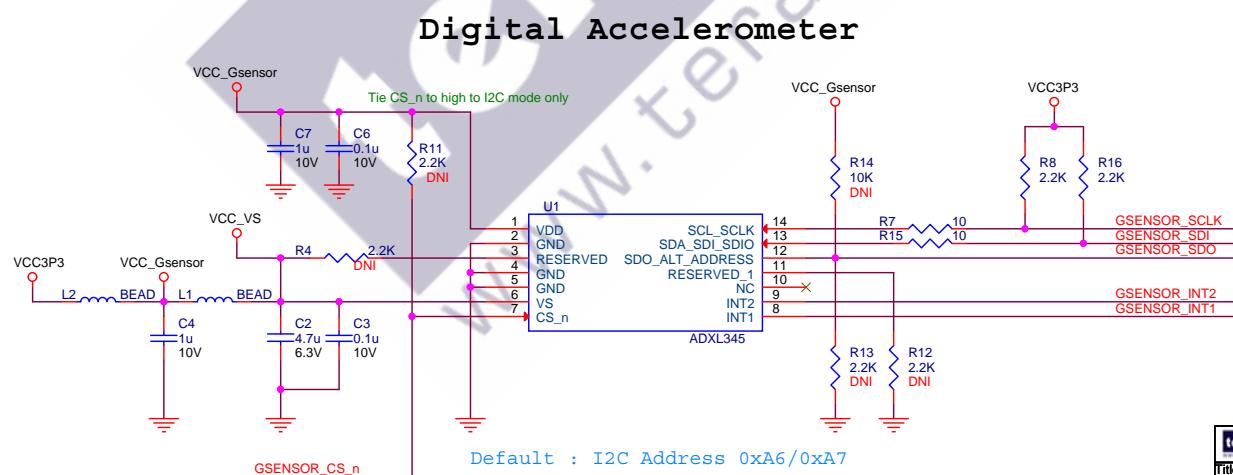
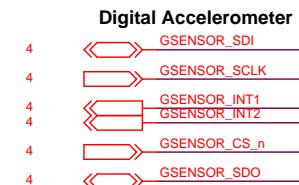
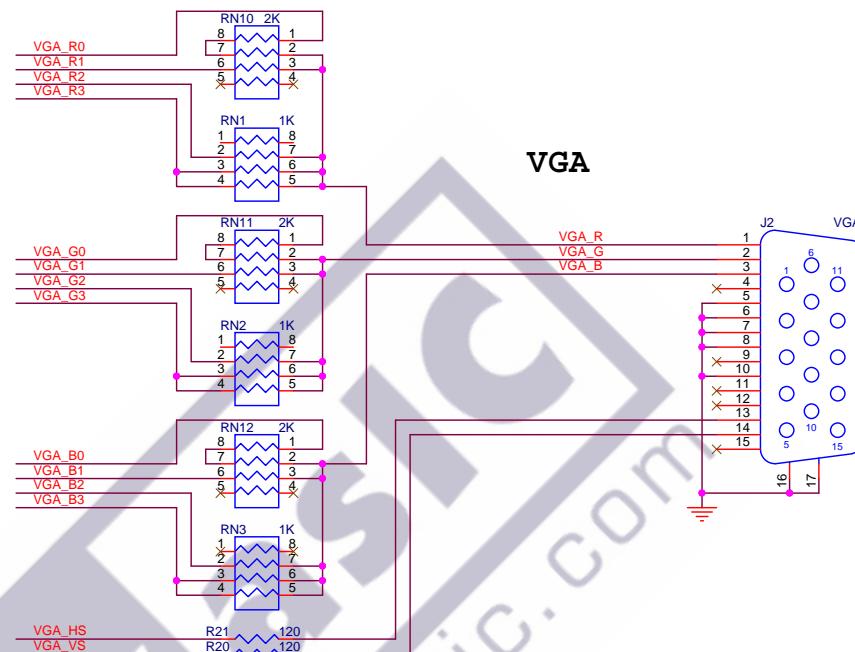
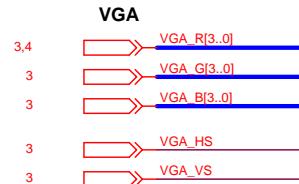
**SWITCH**  
6  
KEY  
6  
LED  
6

**7-segment Display**  
6  
5,6  
5,6  
5,6  
5,6  
5  
5



Copyright © 2017 by Terasic Inc. Taken. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title DE10-Lite	
Size B	Document Number 7Segment, User I/O
Date: Friday, August 04, 2017	Rev E0
Sheet 1	14 of 18

# VGA and Accelerometer



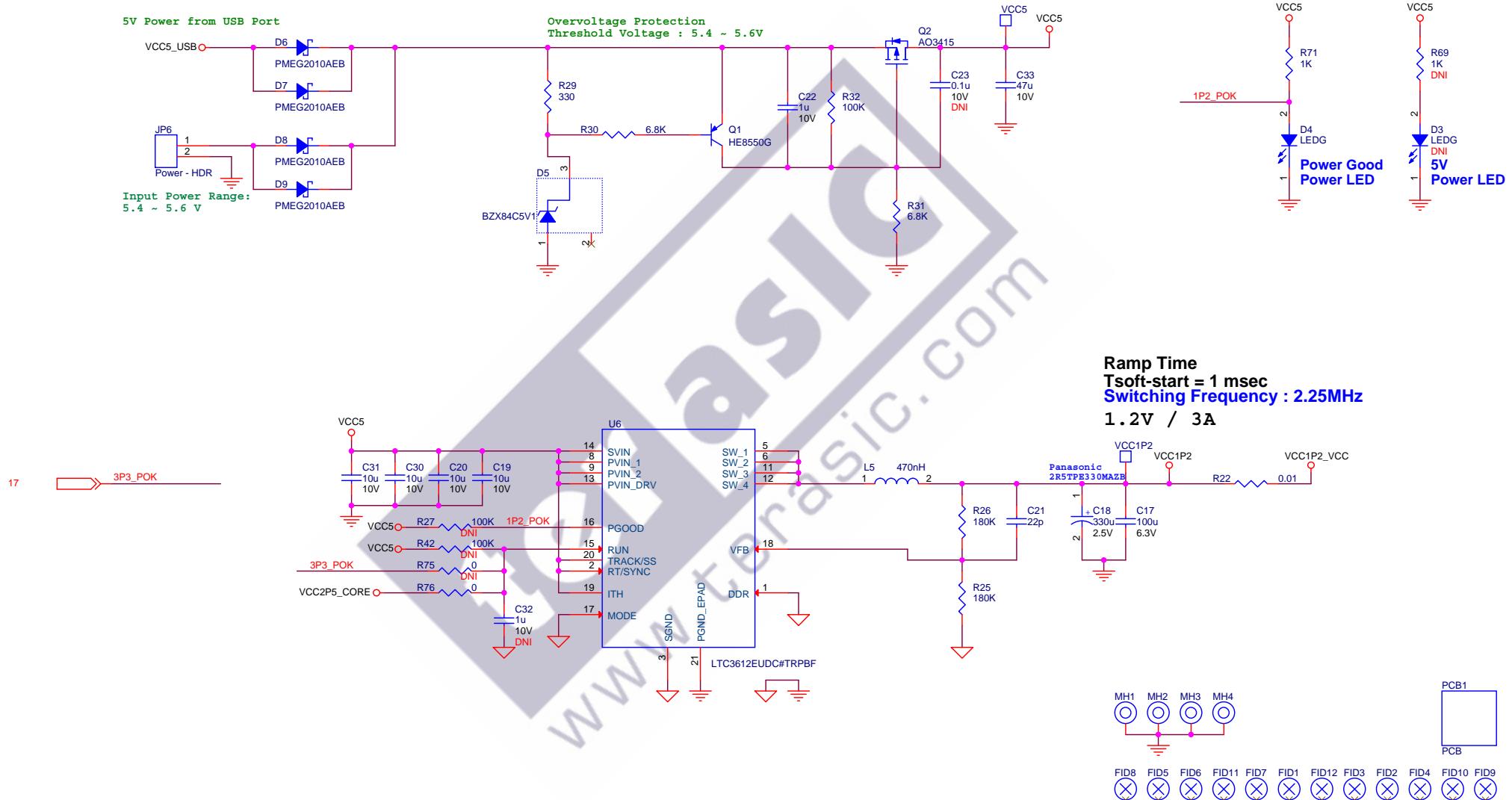
terasic  
Copyright © 2017 by Terasic Inc. All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title	
Size	Document Number
B	VGA and Accelerometer
Rev E0	

Date: Thursday, April 13, 2017 Sheet 1 of 18

# Power - 5V\_DCIN / 1.2V

**Power up Sequence:**  
VCC5 ---> VCC2P5, VCC3P3 ---> VCC1P2\_VCC



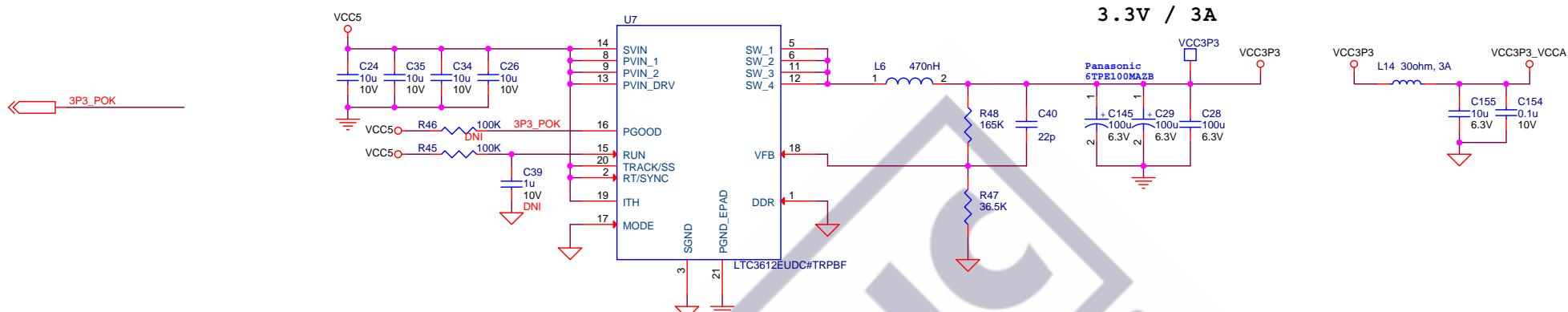
terasic  
Copyright © 2017 by Terasic Inc. Taken.  
All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title	DE10-Lite
Size	Document Number
B	Power - 12V, 5V

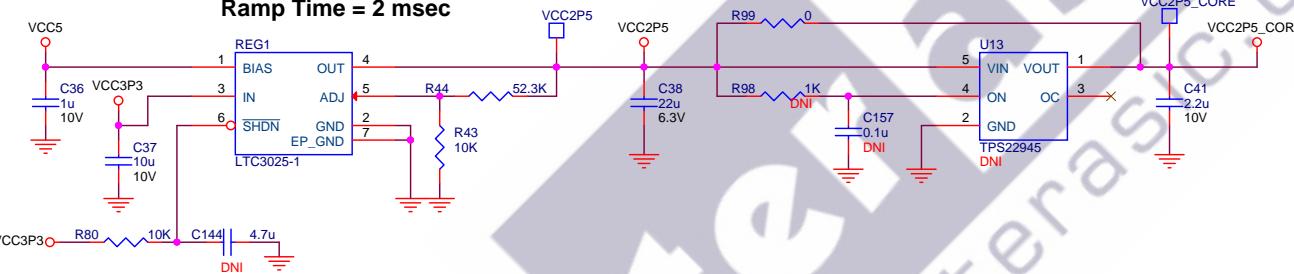
Date: Friday, August 04, 2017 Sheet 16 of 18 Rev E0

# Power - 3.3V / 2.5V

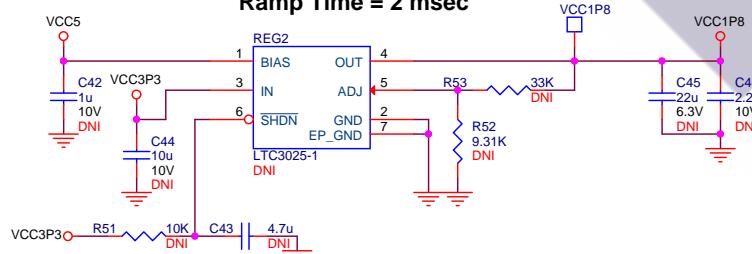
Ramp Time  
Tsoft-start = 1 msec  
Switching Frequency : 2.25MHz  
3.3V / 3A



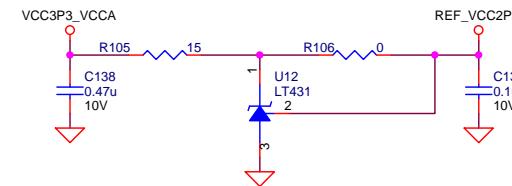
**2.5V / 0.5A**  
Ramp Time = 2 msec



**1.8V / 0.5A**  
Ramp Time = 2 msec



## Voltage Reference



terasic		
Copyright © 2017 by Terasic Inc. All rights reserved.		
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title	DE10-Lite	
Size	Document Number	Rev
B	Power - 1.8V, 2.5V, 3.3V	E0
Date:	Friday, August 04, 2017	Sheet
	1	17 of 18

