



ESP-C3-32S Specification

Version V1.0

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Document development/revision/revocation resume

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1 Product Overview

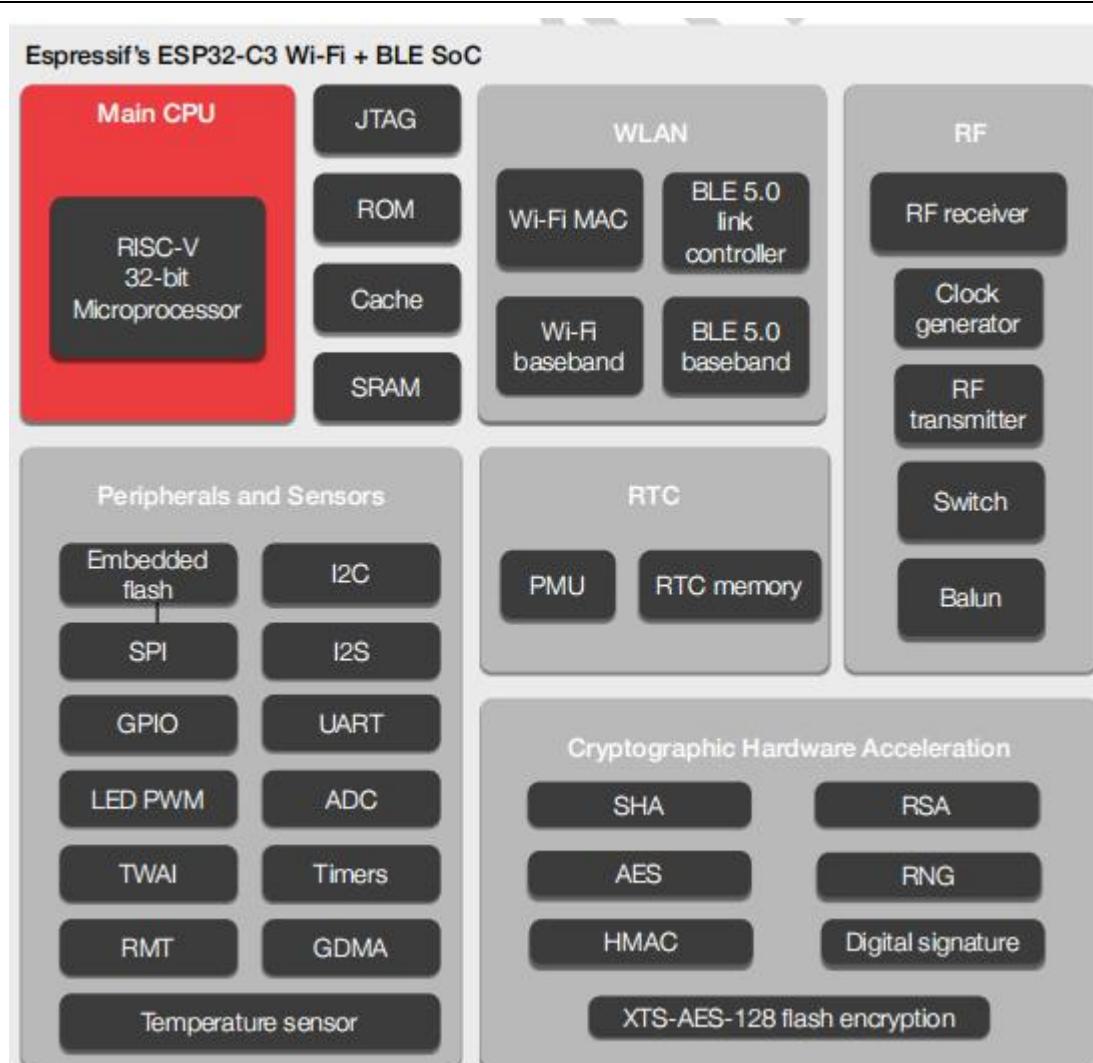
ESP-C3-32S is a Wi-Fi module developed by Ai-Thinker. This module core processor ESP32-C3 is a Wi-Fi+ BLE combination of system-level chips (SoC), designed for various applications such as internet of things (IoT), mobile devices, wearable electronics, smart home, etc.

ESP32-C3 with industry-leading low power and RF performance, supporting Wi-Fi IEEE802.11b/g/n agreements and BLE 5.0. ESP32-C3 chip is equipped with a RISC-V 32-bit single-core processor, operating frequency up to 160 MHz. The chip is support to have secondary development without using other microcontrollers or processors. The chip has a built-in 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM. The chip also support external Flash while it built-in 4Mbit Flash. ESP32-C3 chip supports a variety of low-power consumption working states, which can meet the power consumption requirements of various application scenarios. The chip's unique features such as fine clock gating function, dynamic voltage clock frequency adjustment function, and RF output power adjustable function can achieve the best balance between communication distance, communication speed and power consumption.

ESP-C3-32S module provides a wealth of peripheral interfaces, including UART, PWM, SPI, I2S, I2C, ADC, temperature sensor and there are 21 GPIOs.

ESP-C3-32S has a variety of unique hardware safety mechanisms. The hardware encryption accelerator supports AES、SHA and RSA algorithm. Among them, RNG、HMAC and Digital Signature module provide more security features. Other security features include flash encryption and se-cure boot signature verification, etc. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.

ESP-C3-32S support low-power Bluetooth: Bluetooth5, Bluetooth mesh. Bluetooth rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps. Support broadcast extension, multi-broadcasting, channel selection.



1.1. Characteristics

- Complete Wi-Fi 802.11b/g/n, 1T1R mode data rate up to 150Mbps
- Support BLE5.0 and rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- 32-bit RISC-V single-core processor, supports a clock frequency of up to 160 MHz, with 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM
- Support UART/PWM/GPIO/ADC/I2C/I2S interface, temperature sensor, pulse counter
- SMD-38 package
- Integrated Wi-Fi MAC/ BB/RF/PA/LNA/BLE
- Support multiple sleep modes, deep sleep electric current is less than 5uA
- UART rate up to 5Mbps

- Support STA/AP/STA+AP mode and mix mode
- Support Smart Config (APP)/AirKiss (WeChat) of Android and IOS One-click network configuration
- Support UART port local upgrade and remote firmware upgrade (FOTA)
- General AT commands can be better understand
- Support secondary development, integrated Linux development environment
- ESP-C3-32S module acquiesce in using the built-in 4MByte Flash, meanwhile support external Flash version

1.2. Main parameters

Table 1 main parameter descriptions

Model Name	ESP-C3-32S
Package	SMD-38
Size	25.5*18.0*3.1(± 0.2)mm
Antenna	On-board PCB antenna/IPEX
Frequency Range	2400 ~ 2483.5MHz
Operating Temperature	-40 °C ~ 85 °C
Store Temperature	-40 °C ~ 125 °C , < 90%RH
Power supply range	Supply voltage:3.0V ~ 3.6V, Supply current >500mA
Support Interface	UART/GPIO/ADC/PWM/I2C/I2S
IO	IO0,IO1,IO2,IO3,IO4,IO5,IO6,IO7,IO8,IO9,IO10,IO12,IO13,IO14,IO15, IO16,IO17,IO18,IO19,IO20,IO21
UART Rate	Support 110 ~ 4608000 bps, default 115200 bps
Bluetooth	BLE 5.0
Security	WEP/WPA-PSK/WPA2-PSK
SPI Flash	Default 4MByte, support 2MByte version

2 Electrical parameters

ESP-C3-32S module is electrostatic sensitive devices and special precautions need to be taken when handling



2.1 Electrical characteristics

Parameters	Conditions	Min	Typical values	Max	Unit
Supply voltage	VDD	3.0	3.3	3.6	V
I/O	V _{IL} /V _{IH}	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3
	V _{OL} /V _{OH}	-	N/0.8VIO	-	0.1VIO/N
	I _{MAX}	-	-	12	mA

2.2 WIFI RF performance

Description	Typical values	Unit
Operating frequency	2400 - 2483.5	MHz
Output Power		
11n mode HT40, PA output power	15±2	dBm
11n mode HT20, PA output power	15±2	dBm
11g mode, PA output power	16±2	dBm
11b mode, PA output power	18±2	dBm
Receiving sensitivity		
CCK, 1 Mbps	-96±2	dBm
CCK, 11 Mbps	-88±2	dBm
6 Mbps (1/2 BPSK)	-92±2	dBm

54 Mbps (3/4 64-QAM)	-75±2	dBm
HT20 (MCS7)	-73±2	dBm
HT40 (MCS7)	-70±2	dBm

2.3. WIFI RF performance

Description	Typical values	Unit
Output power		
Transmit power	0±2	dBm
Receiving sensitivity Low Energy consumption BLE: 1M		
Sensitivity@30.8%PER	-96±2	dBm

2.4. Power Consumption

The following power consumption data are based on a 3.3 V power supply, 25°C ambient temperature and measured using an internal voltage regulator.

- All measurements were completed at the antenna interface without SAW filters
- All emission data are based on a duty cycle of 100%, measured in the mode of continuous emission.

Mode	Min	Typical values	Max	Unit
Tx 802.11b, CCK 1Mbps, POUT=+20dBm	-	350	-	mA
Tx 802.11g, OFDM 54Mbps, POUT =+18dBm	-	290	-	mA
Tx 802.11n, MCS7, POUT =+17dBm	-	280	-	mA
Rx 802.11b, 1024 bit	-	90	-	mA
Rx 802.11g, 1024 bit	-	90	-	mA
Rx 802.11n, 1024 bit	-	93	-	mA
Modem-Sleep①	-	20	-	mA

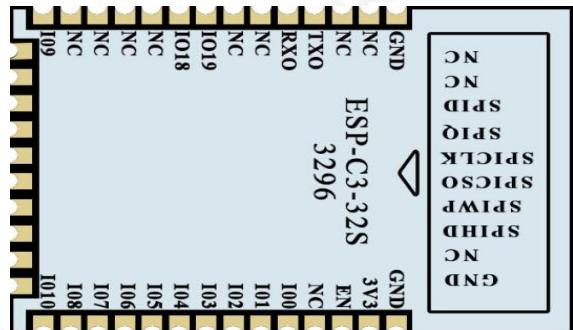
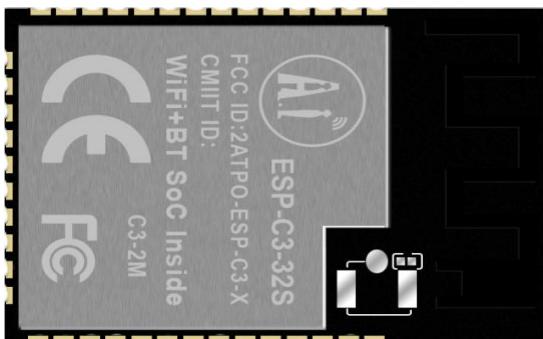
Light-Sleep②	-	130	-	μA
Deep-Sleep③	-	5	-	μA
Power Off	-	1	-	μA

3 Appearance dimensions

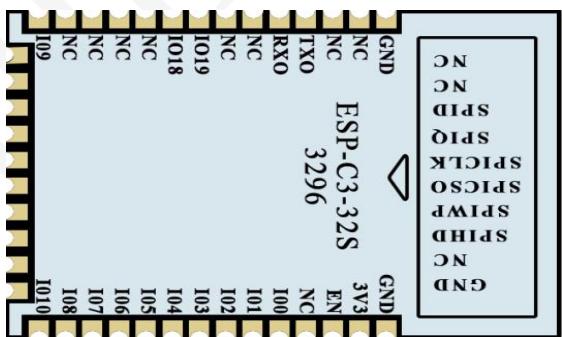
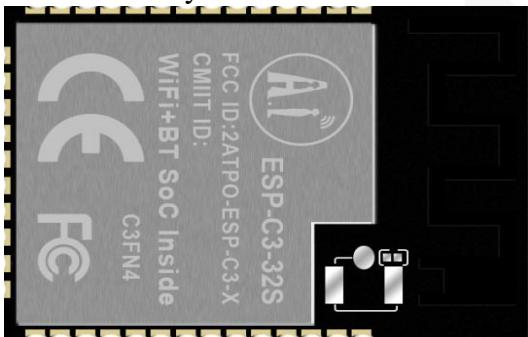
ESP-C3-32S have two FLASH, including external FLASH and build-in FLASH

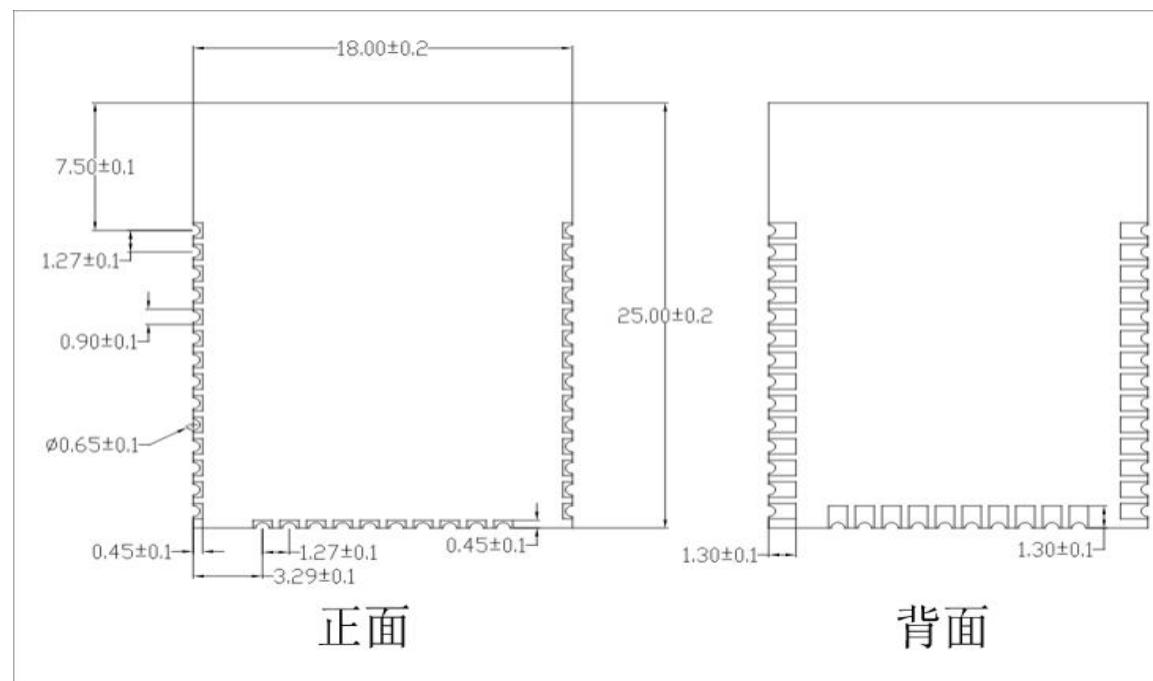
(The rendering is for reference only, the actual product shall prevail)

External 2MByte FLASH:

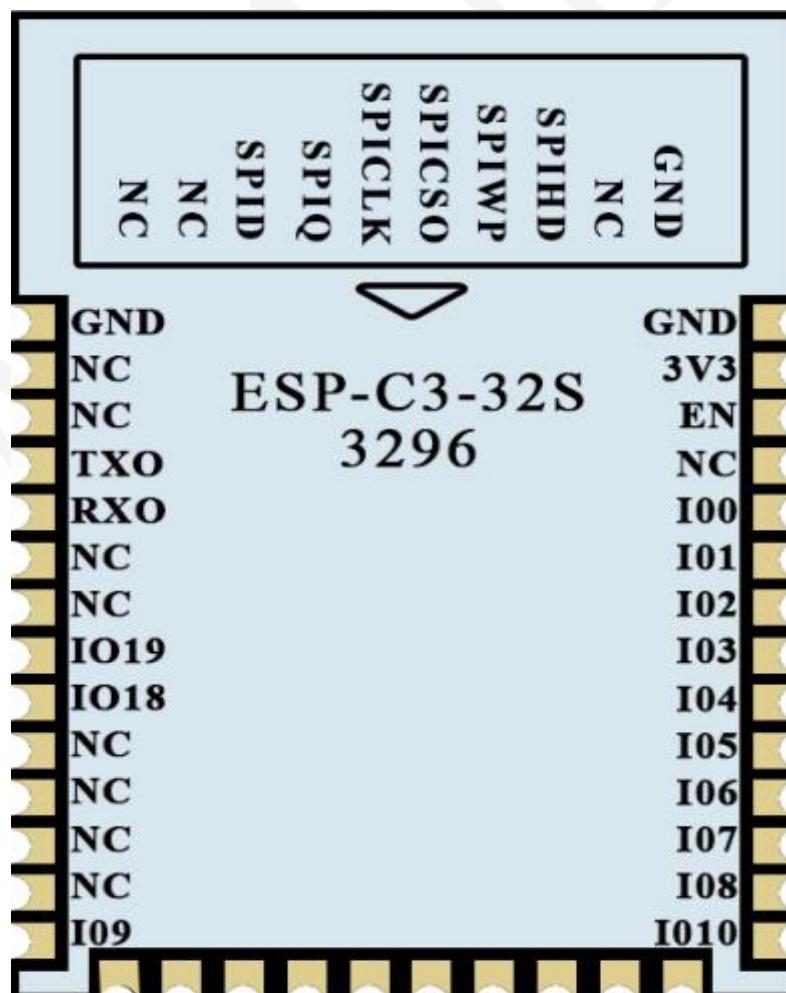


Build-in 4MByte FLASH:





4 Pin definition



 ESP-C3-32S Diagram of Pin

ESP-C3-32S module is connected to 38 interfaces, refer to pin diagram, pin function definition table is interface definition.

ESP-C3-32S Pin function definition

No.	Name	Function
1	GND	GND
2	VCC	VCC
3	EN	High level: chip enabled; Low level: chip shutdown; Pay attention not to leave the CHIP_PU pin floating;
4	NC	NC
5	IO0	GPIO0,ADC1_CH0,XTAL_32K_N
6	IO1	GPIO1,ADC1_CH1,XTAL_32K_N
7	IO2	GPIO2,ADC1_CH2,FSPIQ
8	IO3	GPIO03,ADC1_CH3
9	IO4	GPIO04,ADC1_CH4,FSPIHD,MTMS
10	IO5	GPIO05,ADC2_CH0,FSPIWP,MTDI
11	IO6	GPIO6,FSPICLK,MTCK
12	IO7	GPIO7,FSPIID,MTDO
13	IO8	GPIO8
14	IO10	GPIO10,FSPICSO
15	GND	GND
16	NC	NC
17	SPIHD	SPIHD,GPIO12
18	SPIWP	SPIWP,GPIO13
19	SPICS0	SPICS0,GPIO14
20	SPICLK	SPICLK,GPIO15
21	SPIQ	SPIQ,GPIO17

22	SPID	SPID,GPIO16
23	NC	NC
24	NC	NC
25	IO9	GPIO9
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	IO18	GPIO18
31	IO19	GPIO19
32	NC	NC
33	NC	NC
34	U0RXD	RX0,GPIO20
35	U0TXD	TX0,GPIO21
36	NC	NC
37	NC	NC
38	GND	GND

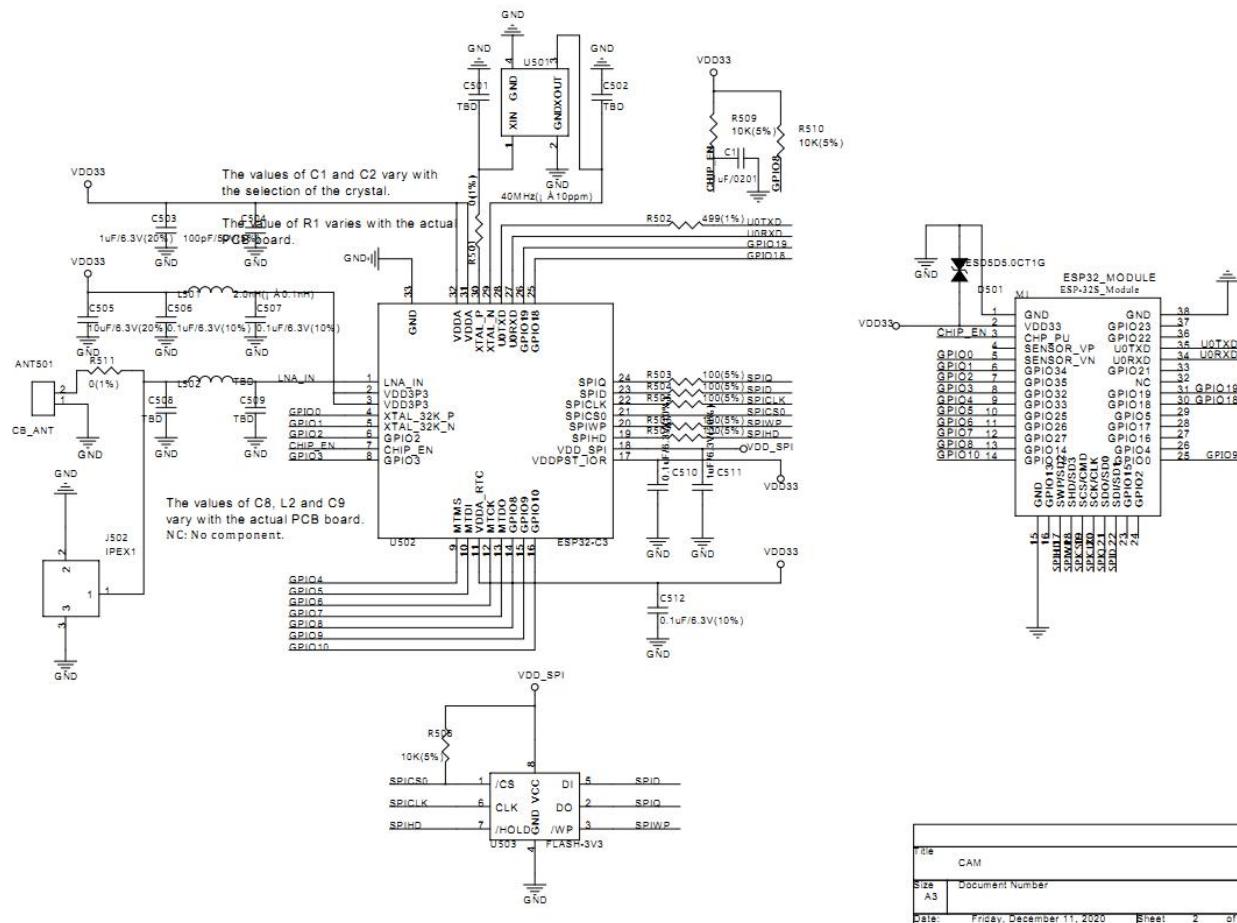
Table Module Start-up Mode Description

System start-up mode			
Pin	Default	SPI Start up mode	Download Start up Mode
IO8	Non	/	1
IO9	Pull up	1	0

Note: Some pins have been internally pulled up, please refer to the schematic

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5 Schematic diagrams



6 Design guidance

6.1. Note:

- (1) When GPIO20 is used as U1RXD, a pull-up resistor needs to be added externally.

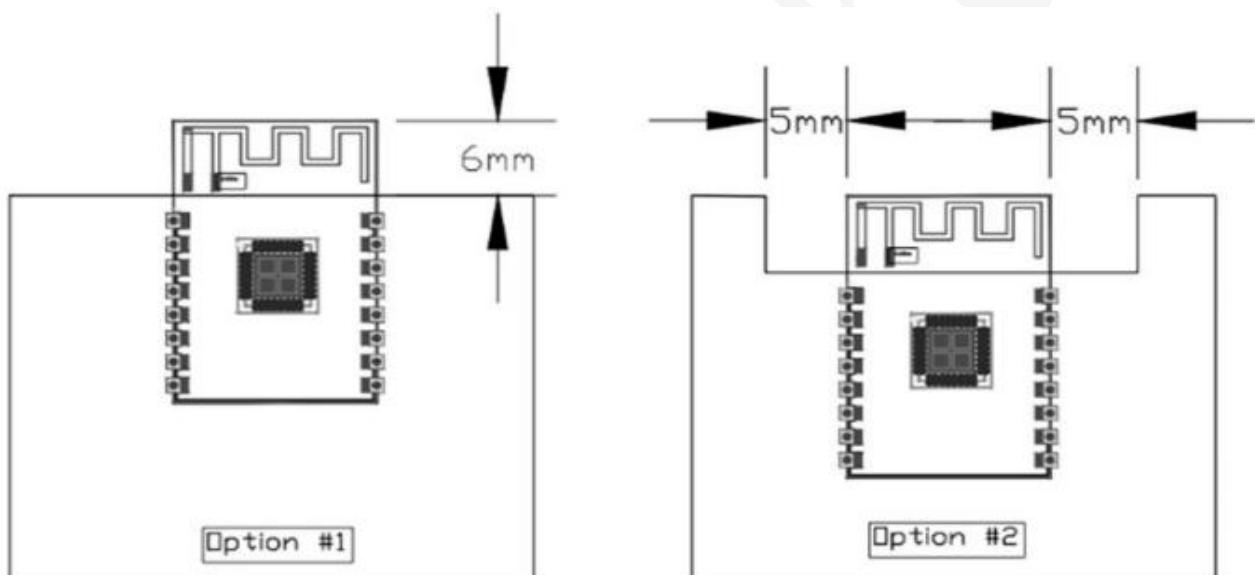
6.2. Antenna layout requirements

(1) For the installation position on the motherboard, the following two methods are recommended:

Solution 1: Put the module on the edge of the main board, and the antenna area extends out of the edge of the main board.

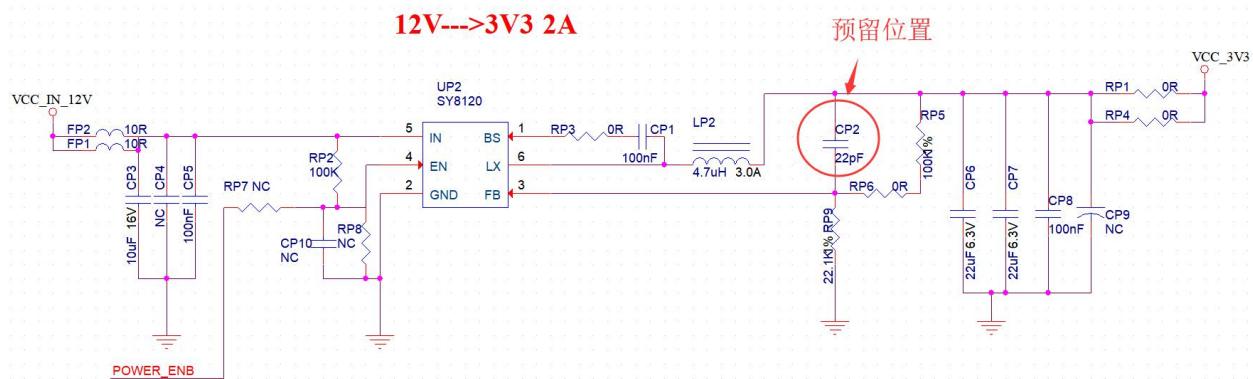
Solution 2: Put the module on the edge of the main board, and hollow out an area at the antenna position on the edge of the main board.

(2) In order to meet the performance of the on-board antenna, metal parts are forbidden to be placed around the antenna, away from high frequency devices.



6.3. Power supply

- (1) Recommend 3.3V voltage, peak current above 500mA
- (2) It is recommended to use LDO for power supply; if DC-DC is used, the ripple is recommended to be controlled within 30mV.
- (3) DC-DC the power supply circuit, it is suggested to reserve the position of output ripple can be optimized when the load changes greatly.
- (4) It is recommended to add ESD devices to the 3.3V power interface.



6.4. GPIO Interface

- (1) The module periphery leads to some GPIO ports, such as the recommended resistance of 10-100 Ohms in series on the IO port. This can suppress overshoot, to ensure both sides of the level more stable. helpful for both EMI and ESD.
- (2) For special IO, please refer to the specification, which will affect the starting configuration of the module.
- (3) The IO port of the module voltage is 3.3 V, if the main control does not match the IO level of the module, require to add the level conversion circuit.
- (4) When the IO port is connected directly to the peripheral interface, or the pin header and other terminals, it is recommended to reserve ESD device near the terminal.

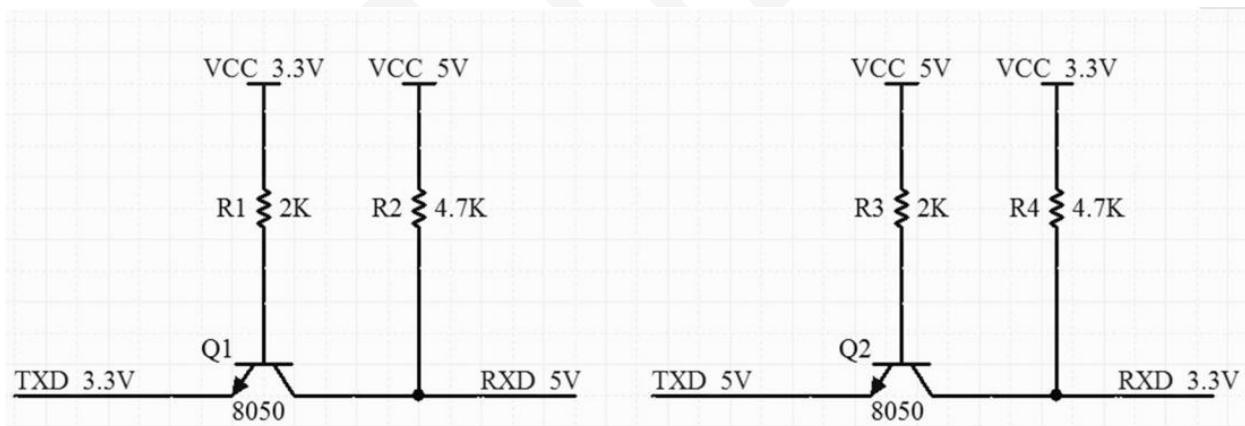
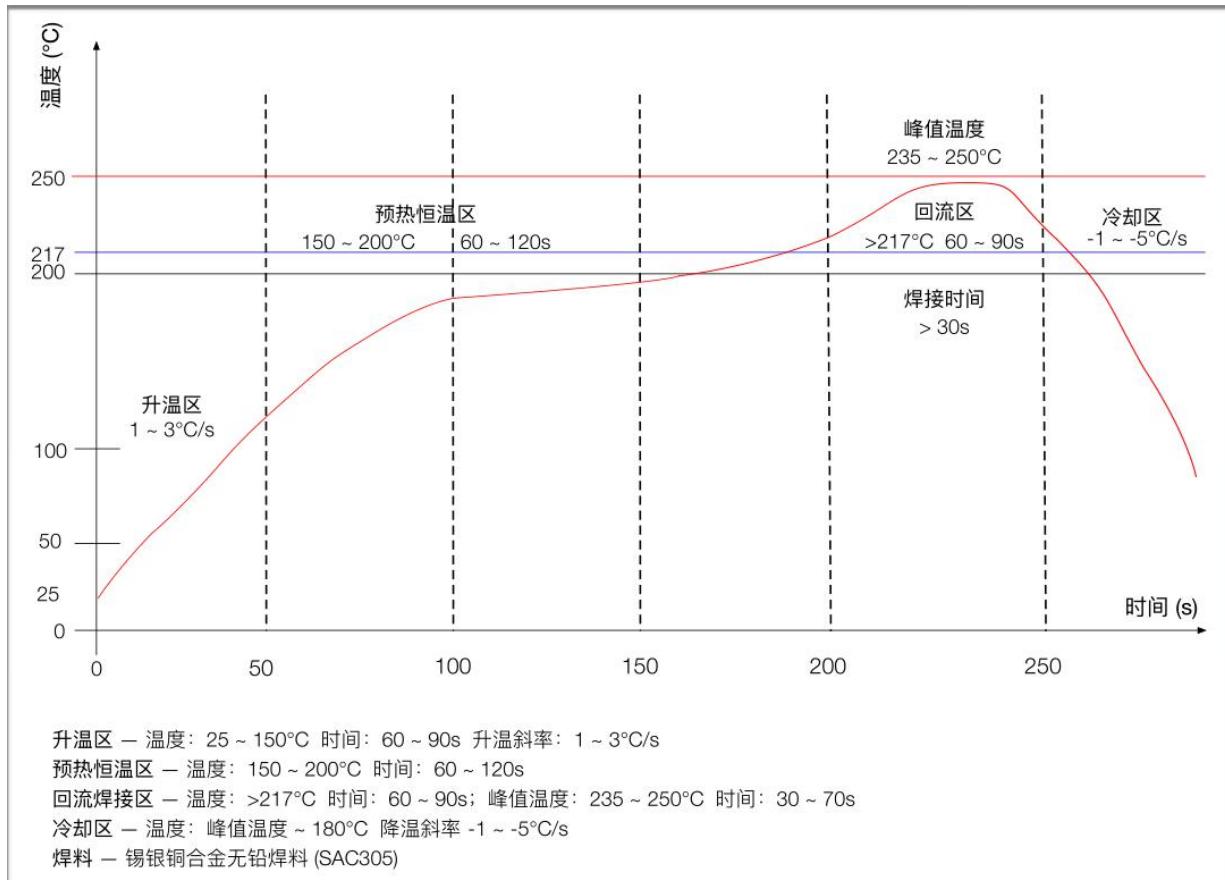


Table Electrical level conversion circuit

7 Reflow soldering



8 Packaging information

Refer to below image, ESP-C3-32S package is in Tape/Reel.



9 Contact us

Official website: <https://www.ai-thinker.com>

Development DOCS: <https://docs.ai-thinker.com>

Official Forum: <http://bbs.ai-thinker.com>

Sample purchase: <https://ai-thinker.en.alibaba.com/>

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